MIPS Updates
“Open Source Software”
August 2012
MIPS Technologies Corporate Snapshot

**Business Overview**

- A leading provider of industry-standard processor architectures and cores
  - A leading position in the digital home
  - Strong in wired and wireless networking
  - Growing position in embedded market
  - Expanding into mobile, with millions of units of smartphones & tablets already shipping

- IP business model—licensing + royalties

- Licensees include Broadcom, Cavium, Loongson, Ingenic, Microchip, MStar, MediaTek, Sony, Toshiba, others

- Valuable portfolio of 570+ patent properties worldwide

- Headquartered in Sunnyvale, CA; presence in 11 countries; approx. 160 employees; more than half in R&D

- >3.6 billion unit installed base since 2000; 708 million units shipped in FY12

**Annual Unit Shipments**

*CAGR 38%*

*MIPS royalty units reflect previous quarter shipments*
MIPS’ Market Presence

Leading Market Share*

Digital TV
Cable, Satellite & IPTV Set-top Boxes
Blu-ray Players
Broadband CPE
WiFi Access Points and Routers

*MIPS and Industry Analyst Data

Leading position in home entertainment; Strong in networking; Aggressively expanding into mobile and embedded
Strategic Growth in Key Market Segments

**Mobile**
- Use Android & 4G to dislodge competition
- Make pioneer customers successful
- Invest in connected device ecosystem

**Home Entertainment**
- Maintain leading position across the home
- Provide leading-edge connected TV solutions for Android and Linux
- Help to define new product categories

**Wired/Wireless Networking**
- Maintain leadership in broadband CPE & WLAN
- Facilitate PowerPC transition to MIPS
- Leverage multicore 64-bit & multi-threading

**Embedded**
- Leverage lead MCU licensee
- Grow ecosystem & leverage partnerships
- Performance efficiency leadership

Maintaining lead in traditional markets; aggressive market expansion
The Cellular Infrastructure and Mobile Spectrum

Infrastructure Connectivity User Equipment

Key Technology Foundation & Ecosystem
- Multicore + Multithread Processors
- WiFi, 4G, GPS, etc.
- >1GHz CPUs
- Android
- Apps and Games

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Multi-core processors (MIPS64) from Cavium & NetLogic; NPUs from PMC-Sierra drive growth in Infrastructure
- Design-ins for eNBs/BTS/RNC for 4G & 3G
- New “Fusion” small cell SoC from Cavium

Growing presence in 3G/4G baseband
- Millions of units shipped in CY11

Leading share in WLAN infrastructure
- 60%+ share in wireless access points & routers
Mobile momentum continues with new ecosystem developments and new products in the market.
Android on MIPS Timeline

- 2009: MIPS brings Android beyond mobile
- 2010: Android STB ships to market
- 2011: Google licenses Honeycomb to MIPS
- First Android 4.0 ICS tablets worldwide, It’s MIPS!
- 2012: Philips launches 100% CTS certified MIPS tablets in China
World’s First Available Android 4.0 Tablet
— Yes it’s MIPS!

“I’m thrilled to see the entrance of MIPS-Based Android 4.0 tablets into the market. Low cost, high performance tablets are a big win for mobile consumers and a strong illustration of how Android’s openness drives innovation and competition for the benefit of consumers around the world.”

—Dec 5th, 2011,
Andy Rubin,
Senior Vice President of Mobile,
Google

✓ Android 4.0 – Ice Cream Sandwich
✓ Full functionality
✓ 1GHz performance
✓ Low power consumption
✓ Low cost: ASP below $100!
✓ Android 4.0.3 reference port available at developer.mips.com

2 weeks after Google released Android 4.0, MIPS led the market by announcing availability of first ICS tablet
New Philips T7/T7+ Tablet: it’s MIPS!

First non-ARM Android 4.0 Devices to Pass Android Compatibility Test Suite (CTS)
GOOGLE OFFICIALLY SUPPORTS MIPS IN ANDROID
On 7/31/12 MIPS announced the world’s second JB tablet

- Sells for about $125 in India
- “… With our deep expertise in Android development, we are able to quickly port new versions of Android to MIPS-Based devices, with speed that is second only to Google itself”
More Mobile Momentum in FY12

- Multiple tablet OEMs in six months!
  - Ainol (Ainovo), K-touch, Speedup, Philips, Karbonn
  - Millions of devices shipped last year

- Actions Semiconductor 74Kf based SoC in Ramos tablets coming soon

- Complete support for MIPS ABI in Google’s NDK

- MIPS was part of Google’s Platform Development Kit for “Jelly Bean”

- Altair and Sequans shipping state-of-the-art 4G LTE solutions based on MIPS

- NationZ shipping NFC solutions based on MIPS
  - More than one million units already shipped!
Mobile Momentum – Looking towards FY13

- **MIPS Jelly Bean sources available on developer.mips.com**
- **All of MIPS Android sources submitted to Google**
  - Next release of Android expected to support MIPS 100% on day 1 of going open source
- **Next release of Android SDK to include MIPS emulator, ICS and JB system images**
- **Delivering ARM to MIPS binary translator (MagicCode) to customers (available on developer.mips.com)**
  - Customers successfully integrated and is able to hit 70% ARMv5 translation to MIPS success
- **Next release of Google Play to include multiple APK support**
  - Includes MIPS ABI being default for native application development
Mobile Momentum – 3rd Party Support

- Gameloft to release 20 game titles
- Marmalade and Yoyo cross-toolchain support
- Rightware (Basemark GUI, Basemark OS, Basemark ES) available
- Xamarin (.net framework for linux) supports MIPS
- World’s most popular browser, Opera Mobile: 100% MIPS support
- Halfbrick, maker’s of popular “Fruit Ninja” to support MIPS
Downstream Business Development in Mobile

- MIPS has a proven track record of facilitating (technical, marketing and PR) launches of successful devices
  - Speedup launched in Indonesia in four months from first meeting
  - Philips launched in China in four months from first meeting
  - Ainovo shipped the world’s first ICS tablet
  - 3G/4G reference designs underway

- MIPS has very high credibility within Google, to help deliver fast, aggressive results
  - CTS experience, Widevine knowledge, etc.
  - Up-to-date and timely submissions and patches to AOSP
The Importance of Emerging Markets

- **No dominant tablets or smartphones in emerging markets (e.g. China, Indonesia, Brazil, India, Thailand, Brazil and others)**
  - With lower levels of disposable income, devices targeted for developed markets are out of reach for most consumers
  - Significant demand exists if devices have the right price/performance point

- **MIPS enables the “sweet spot” in these markets**
  - Highly-scalable architecture with excellent software platforms
  - Brand name recognition: legendary performance and power efficiency
  - Lower total cost of ownership with small silicon footprint + flexible business model

- **MIPS-Based silicon enables OEMs to create attractive, differentiated solutions**
  - High-performance, feature-rich, high-quality devices
  - Price + capabilities = compelling competitive advantage
  - Appealing, affordable products ultimately benefit consumers worldwide

MIPS’ performance-efficient products are “right sized” for emerging markets; poised to drive mass adoption
MIPS: the Credible Alternative for Mobile

Technology

- Efficiency of MIPS architecture delivers high performance with compact area, and low power consumption
- Multi-threading technology can provide significant additional benefits
- MIPS architecture delivers the connected multimedia experience

Ecosystem

- Working closely with Google to quickly enable the latest releases of Android –the world’s first Android 4.0 tablet is MIPS!
- Bringing the most popular Android apps and games to MIPS
- Best-in-class hardware and software IP partners

Business

- Consumer-focused model, providing the right level of performance with low power consumption and lower total cost of ownership
- Partnering with our customers for mutual success
- Bringing the leading consumer entertainment experience of MIPS to the mobile world
Access to any Content, any Time, Anywhere

MIPS: the architecture of choice for the Converged Consumer Experience
MIPS Shipping in all Major Brands in Digital Home
MIPS-Based Smart TVs in Volume Production

- Konka, Skyworth, TCL, Hisense and other mainstream TV manufacturers ramping up Android TV production
Multi-Screen Integration

Smart devices are becoming complementary, integrated/extended systems
The Future of Multi-Screen Entertainment

TV Channel Preview on a Mobile Device

Enhanced Second Screen TV Integration
- Remote DVR
- STB at the center of the content experience
- Mobile Content Experience
- Advanced Instant Replay
- Multi-camera views

Social Gaming in home or over social networks
iPPea TV: Smart TV for the Masses

- Makes any HDMI-enabled DTV a Smart Connected TV
- Full Connected HD Entertainment Experience
  - Access Internet-based movies, music, and photos
- Brings full Android 4.0 to the TV
  - Take advantage of the Android ecosystem
- Extremely low power
  - <$50
MIPS focus within a Linux system
Software Architectures
Cross Platform Compatibility - Native Performance

Web Browsing
- JavaScript engine
- WebGL
- CPU
- GPU

Android Applications
- Dalvik JIT
- OGL ES 2
- CPU
- GPU

Flash 11 Video & Gaming
- Actionscript 3 engine
- Stage3D
- CPU
- GPU

HTML 5 Web Applications
- Portable Native Client
- WebGL
- CPU
- GPU

Android
- Renderscript Compute
- Renderscript Graphics
- CPU
- GPU

Cross Platform Gaming
- Portable Native Client
- WebGL
- CPU
- GPU

MIPS processor optimizations available now for web technologies!
The Future of Application Portability - LLVM

Hardware independent application development

Objective C
C
C++
Java
OpenGL
Renderscript

LLVM Front End (e.g. Clang)

LLVM IR
bitcode

LLVM JIT

CPU
GPU
DSP

Device

Application Development

LLVM JIT handles device specific optimizations

MIPS officially supported in LLVM v3.0
ARCHITECTURE AND PRODUCTS
The Heritage of the MIPS Architecture

Pioneered by Stanford President John Hennessy in the 1980s

Pure, fast, efficient, elegant RISC architecture designed for performance

Now the architecture of choice for multimedia, home networking & beyond

Innovation continues by MIPS and architecture licensees—Broadcom, Cavium, Loongson, Ingenic, Renesas, Toshiba, others

Strong patent position with more than 570 patent properties worldwide

Widely used, widely taught architecture with millions of lines of code written for it

Photo: In 1984, Stanford computer scientists John Shott, John Hennessy and James D. Meindl brainstorm about the MIPS project (Photo: Chuck Painter)
A Systematic Philosophy for Design Success

Foundation for Success Built on MIPS’ Legacy of Scalability

- 1991: Industry’s First 64-bit Microprocessor
- 1999: MIPS32 and MIPS64 Architectures
- 2001: Highest Performance, Synthesizable, Licensable 32-bit Cores
- 2002: Microcontroller-specific Cores
- 2005: DSP Extensions
- 2006: Multi-threading
- 2007: Superscalar Performance
- 2008: Coherent Multiprocessing
- 2010: microMIPS Advanced Code Compression
- 2012: microMIPS Advanced Code Compression

Efficiency and Performance
Industry’s Most Scalable Processor Architecture

Microchip PIC32 Microcontrollers

64-bit Multicore Chips for Advanced Networking

And everything in between
**Benefits of Multi-core and Multi-threading**

- **Benefits of Multi-core and Multi-threading shown on Android browser**
  - EEMBC Engineering Subset of BrowsingBench™ workload shown

- **Benefits of more threads**
  - Second core increases performance by 2X
  - Second thread, or virtual processing element (VPE) increases performance ~40%
  - For a given performance level, MT generally allows operation at lower frequencies and lower dynamic power
  - MT also saves static power and die cost since it adds less area than a full core

---

No special instrumentation of software: Simply declared each VPE on the processor as an independent core!!
Welcome to the Aptiv™ Generation

Don’t just think it. Do it. Get Aptiv!
MIPS32® Processor Core Portfolio

**Classic MIPS Products**

- **MIPS32 Processor Core Portfolio**
  - **M14K/c Series**
    - 5 stage pipeline
    - MCU/MPU microMIPS ISA
  - **M4K/4KE Series**
    - 8-stage pipeline with DSP ASE
  - **34K Series**
    - Multi-threaded 9-stage pipeline
  - **1004K Series**
    - Multi-threaded core, high-performance CM+L2$ (1 ➔ 4 core versions)
  - **24K/24KE Series**
    - Out of Order (OoO) Dual issue CPU (1 ➔ 6 core versions)
  - **74K Series**

**Aptiv™ Generation**

- **proAptiv™ Family**
  - Per Core:
    - 4.5 CoreMark/MHz
    - 3.5 DMIPS/MHZ
  - Bonded triple-dispatch superscalar Out-of-Order CPU
  - Enhanced Virtual Address (EVA), high-speed FPU, high-performance CM+L2$
  - 1 ➔ 6 core versions

- **interAptiv™ Family**
  - Per Core:
    - 3.2 CoreMark/MHz
    - 1.7 DMIPS/MHZ
  - Multi-threaded core, ECC, EVA, low power, high-performance CM+L2$
  - 1 ➔ 4 core versions

- **microAptiv™ Family**
  - Real-time CPU with DSP and SIMD for microcontrollers and deeply embedded applications
  - 3.1 CoreMark/MHz
  - 1.57 DMIPS/MHZ
MIPS APTIV CORES HIT THE MARK

New Family Shows Highest CoreMark/MHz for Licensable CPUs

“For now, the MIPS design team seems to have taken the performance lead away from ARM, and it deserves credit for this accomplishment.”

– May 28, 2012

J. Scott Gardner, Senior Analyst at The Linley Group, senior editor for Microprocessor Report

Full article is available for download at: http://www.mips.com/media/files/aptiv/Aptiv_Cores_Hit_the_Mark.pdf
Competitive Per Core Performance – Half the Size

Dual Core Cortex A15 size ~ Quad Core proAptiv size

<table>
<thead>
<tr>
<th>@ 1.0 GHz</th>
<th>proAptiv Quad</th>
<th>Cortex A15 Dual</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total DMIPS</td>
<td>14,000</td>
<td>7,000</td>
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No specific process or implementations conditions included in above target frequency, but readily achievable in 40G and 28HPM on both processors, and area assumes common process node.

Cortex A15 info – Estimated area, no public info for this core is provided by ARM.
proAptiv Delivers High End Performance Efficiently

**proAptiv** vs. A15

**Equal DMIPS @ nearly ½ the size!**

**proAptiv = top CoreMark score in Industry!**

- **26% higher than Cortex A15**

**proAptiv -> performance architecture with sophisticated branch prediction**

- proAptiv results: prelim/target PPA specs + measured benchmarks on FPGA bitfile of pre-GA RTL
- Cortex A15 CoreMark results as estimated by Microprocessor Report
interAptiv CoreMark Advantage

All implementations consume similar silicon area

@ 800 MHz

interAptiv CoreMark performance leadership!

<table>
<thead>
<tr>
<th>Implementation</th>
<th>DMIPS</th>
<th>CoreMark</th>
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<tbody>
<tr>
<td>Cortex-A5 (x3)</td>
<td>4000</td>
<td>5000</td>
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<tr>
<td>Cortex-A7 (x3)</td>
<td>3000</td>
<td>4000</td>
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<tr>
<td>Cortex-A9 (x2)</td>
<td>2000</td>
<td>3000</td>
</tr>
<tr>
<td>interAptiv (x3)</td>
<td>1000</td>
<td>DMIPS</td>
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<tr>
<td>A7 CoreMark Score?</td>
<td>9000</td>
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interAptiv exceeds same-class Cortex devices on a CoreMark/MHz per core and CoreMark/mm² basis

1. ARM = 12T power opt, MIPS = 12T area opt to 800 MHz freq, worst case SS corner with production margins
2. Product configs include cores with FPU, 32KB Inst/Data L1$, coherence fabric, IO coherence, L2$ (no L2 RAM) and debug logic
3. Source: MIPS and ARM public data; A9 area estimated from published 4.6mm² data and floorplan, with Neon area removed
microAptiv vs. Cortex-M4 Performance

Comparing DSP performance (higher is better)
microAptiv DSP Library, Cortex M4 CMSIS Library
**Strategic Ecosystem in Place**

**Complementary IP and Enabling Technologies**

<table>
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<tr>
<th>Graphics</th>
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<td>Video</td>
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<td>Design Services</td>
<td>RTOS</td>
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</table>

**Wireless Stacks**

- InterDigital
- 4M WIRELESS
- TATA ELXSI LIMITED
- L&T Infotech

**Development Tools**

- CoreSource
- Imperas
- Mentor Graphics
- Open Source Initiative
- Synopsys
- LLVM

**EDA/ESL**

- Xilinx
- Cadence
- Mentor Graphics
- Magma
- Xilinx
- Mentor Graphics
- Xilinx

**Apps, Games, Web**

- Google
- Xamarin
- Qt
- Opera
- Mozilla

**Industry Orgs**

- Foss Foundations
- Open Handset Alliance
- The Linux Foundation
- CE Linux Forum

**Support for MIPS built over 20+ years**
Aptiv Cores Span a Broad Application Range

Mobile
- High-end smartphone & tablet apps processor

Home Entertainment
- High-end DTV/STB/BD processor

Networking
- Res. Gateway
- 802.11ac
- 3G/4G cellular infrastructure

Embedded
- Automotive infotainment

proAptiv™
- Low-to mid-range apps processor
- LTE baseband controller

interAptiv™
- Mainstream DTV/STB/BD processor
- Digital camera

microAptiv™
- Touchscreen
- SIM/security
- GPS

- Conditional access
- WHDMI

- Broadband CPE
- Femtocell
- Smart gateway
- NAS

- Auto collision avoidance
- Auto powertrain
- SATA/RAID/SSD

- VoIP
- MOCA
- WLAN

- MCU
- Industrial
- Smart meters
- Automotive body/chassis

- Auto collision
- Auto powertrain
- SATA/RAID/SSD

- VoIP
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- WLAN

- MCU
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- Automotive body/chassis
Why MIPS? Why Now?

Corporate

• >3 billion unit installed base since 2000; 708 million units in FY12
• Debt-free; over $110 million cash in bank as of 6/30/12
• Strong patent position with more than 570 patent properties worldwide

Markets

• Strong in networking and home entertainment; leading share in DTV, set-top boxes, broadband CPE, WLAN access points/ routers
• Aggressively expanding into mobile: millions of smartphones and tablets shipped to-date

Technology

• More scalable and efficient architecture than the competition: low power consumption and low cost with right-sized performance
• 20+ years’ experience in 64-bits—broad ecosystem of support
• Multi-threading provides unique benefits for numerous applications
Thank You

At the core of the user experience®